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| APPLICATION NO.   | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO.       | CONFIRMATION NO.       |
|---|-------------|----------------------|---------------------------|------------------------|
| 10/811,107  | 03/26/2004  | Hironobu Fukui       | 2102475-992050            | 9214                   |
| 26379   | 7590        | 08/24/2007           |                           |                        |
| DLA PIPER US LLP<br>2000 UNIVERSITY AVENUE<br>E. PALO ALTO, CA 94303-2248 |             |                      | EXAMINER<br>LEWIS, MONICA |                        |
|   |             |                      | ART UNIT<br>2822          | PAPER NUMBER           |
|   |             |                      | MAIL DATE<br>08/24/2007   | DELIVERY MODE<br>PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

## Office Action Summary

Application No.

10/811,107

Applicant(s)

HIRONOBU FUKUI

Examiner

Monica Lewis

Art Unit

2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 04 June 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) 5-20 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-3 is/are rejected.
- 7) ☒ Claim(s) 4 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
  - 2) ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date 3/04.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_.

### DETAILED ACTION

1. This office action is in response to the election filed June 4, 2007.

#### *Election/Restrictions*

2. Applicant's election without traverse of Embodiment I in the reply filed on 6/4/07 is acknowledged.

#### *Specification*

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

#### *Claim Rejections - 35 USC § 102*

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Fujitsu (Japanese Publication No. 07086418).

In regards to claim 1, Fujitsu discloses the following:

a) an additional load capacitance that is formed at a part of the semiconductor device, which is vulnerable to soft errors (For Example: See Abstract)(Note: Applicant disclosed that “an increase in junction capacitance is equivalent to the increase in load capacitance (For Example: See Page 8 Lines 12-15)).

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In regards to claim 2, Fujitsu discloses the following:

a) the part that is vulnerable to soft errors is a first diffusion layer region (9), and the first diffusion layer region is at least a part of diffusion layer regions formed in the MOS type transistor structure and is connected to neither a power supply nor a ground (For Example: See Abstract and Figure 1).

In regards to claim 3, Fujitsu discloses the following:

a) the formation of the additional load capacitance is performed such that a well region (7) that is formed immediately below the first diffusion layer region is made to have higher concentration than other well region (2) (For Example: See Abstract and Figure 1).

6. Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Jerome et al. (U.S. Patent No. 4,903,087).

In regards to claim 1, Jerome et al. ("Jerome") discloses the following:

a) an additional load capacitance that is formed at a part of the semiconductor device, which is vulnerable to soft errors (For Example: See Derwent Abstract)(Note: Applicant disclosed that "an increase in junction capacitance is equivalent to the increase in load capacitance (For Example: See Page 8 Lines 12-15)).

In regards to claim 2, Jerome discloses the following:

a) the part that is vulnerable to soft errors is a first diffusion layer region (34), and the first diffusion layer region is at least a part of diffusion layer regions formed in the MOS type transistor structure and is connected to neither a power supply nor a ground (For Example: See Abstract and Figure 4).

In regards to claim 3, Jerome discloses the following:

a) the formation of the additional load capacitance is performed such that a well region (12) that is formed immediately below the first diffusion layer region is made to have higher concentration than other well region (15) (For Example: See Figure 4).

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7. Claims 1 and 2 are rejected under 35 U.S.C. 102(e) as being anticipated by Nakazato et al. (U.S. Patent No. 6,740,958).

In regards to claim 1, Nakazato et al. ("Nakazato") discloses the following:

a) an additional load capacitance that is formed at a part of the semiconductor device, which is vulnerable to soft errors (For Example: See Column 11 Lines 32-61)(Note: Applicant disclosed that "an increase in junction capacitance is equivalent to the increase in load capacitance (For Example: See Page 8 Lines 12-15)).

In regards to claim 2, Nakazato discloses the following:

a) the part that is vulnerable to soft errors is a first diffusion layer region (10), and the first diffusion layer region is at least a part of diffusion layer regions formed in the MOS type transistor structure and is connected to neither a power supply nor a ground (For Example: See Column 11 Lines 32-61 and Figure 1).

***Claim Rejections - 35 USC § 103***

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakazato et al. (U.S. Patent No. 6,740,958) in view of Fujitsu (Japanese Publication No. 07086418).

In regards to claim 3, Nakazato fails to disclose the following:

a) the formation of the additional load capacitance is performed such that a well region that is formed immediately below the first diffusion layer region is made to have higher concentration than other well region.

However, Fujitsu discloses that the formation of the additional load capacitance is performed such that a well region that is formed immediately below the first diffusion layer region is made to have higher concentration than other well region (For Example: See

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Abstract and Figure 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Nakazoto to include that the formation of the additional load capacitance is performed such that a well region that is formed immediately below the first diffusion layer region is made to have higher concentration than other well region as disclosed in Fujitsu because it aids in improving the reliability of the device (For Example: See Abstract).

Additionally, since Nakazoto and Fujitsu are both from the same field of endeavor, the purpose disclosed by Fujitsu would have been recognized in the pertinent art of Nakazoto.

***Allowable Subject Matter***

10. Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Conclusion***

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 571-272-1838. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-272-8300 for regular and after final communications.

ML  
August 20, 2007

  
**MONICA LEWIS**  
**PRIMARY PATENT EXAMINER**